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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,296	06/22/2001	David A. Fotland	20880-06029	9976

758 7590 10/05/2005

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,296	FOTLAND ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *12-19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/14/05, 9/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. The restriction of claims 12-19 from claims 1-11 is maintained for the reasons set forth below.

2. According to MPEP 806.05(c) I,

SUBCOMBINATION NOT ESSENTIAL TO COMBINATION
AB br /B sp Restriction Proper

Where a combination as claimed does not set forth the details of the subcombination as separately claimed and the subcombination has separate utility, the inventions are distinct and restriction is proper if reasons exist for insisting upon the restriction; i.e., separate classification, status, or field of search.

This situation can be diagramed as combination Abbr ("br" is an abbreviation for "broad"), and subcombination Bsp ("sp" is an abbreviation for "specific"). Bbr indicates that in the combination the subcombination is broadly recited and that the specific characteristics set forth in the subcombination claim Bsp are not set forth in the combination claim.

Since claims to both the subcombination and combination are presented and assumed to be patentable, the omission of details of the claimed subcombination Bsp in the combination claim ABbr is evidence that the patentability of the combination does not rely on the details of the specific subcombination.

3. Claims 1-11 are the combination claims, which have broadly claimed the details of the control status register. Claims 12-19 are the subcombination claims that have specifically claimed details of the control status register, with a separate utility of having the control status register control where the source and/or destination data are transferred from and/or to by using overriding bits, which is properly classified in 712/225. The details of the control status register claimed in subcombination claims 12-19 are not required of combination claims 1-11 as evidenced by the lack of the details in claim 1-11. Therefore the restriction is proper.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-4, 5, 6, 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "the first control status register" in lines 27 and 28. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 1 recites the limitation "the second control status register" in lines 29 and 30. There is insufficient antecedent basis for this limitation in the claim.

8. Claims 2-4 are rejected for incorporating the defects of claim 1.

9. Claim 6 recites the limitation "the context" in lines 2-4. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 9 recites the limitation "the context" in line 2. There is insufficient antecedent basis for this limitation in the claim.

11. Claim10 is rejected for incorporating the defects of claim 9.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al., U.S. Patent Number 6,542,991 (herein referred to as Joy).

14. Referring to claim 1, Joy has taught a multithreaded computer based system for enabling a command in a first thread to accessing data in a second thread comprising:

a. an embedded pipelined processor capable having a first program thread and a second program thread in an execution pipeline, said first program thread comprising a first set of instructions, said second program thread comprising a second set of instructions (Joy, abstract, Figure 3, column 2 line 58-column 3 line 2, Figure 8, column 8 lines 45-58), said embedded processor comprising:

b. a fetch unit for fetching an instruction from program memory (Joy, Figure 12, element 1216);

c. a decode unit for decoding said fetched instruction (Joy, Figure 12, element 1214);

d. an execution unit for executing said decoded instructions (Joy, Figure 12, elements1232, 1234, 1236, 1238, 1240, 1242, 1244, 1246);

e. a write back unit for writing the results of said executed instruction to an identified storage location (Joy, Figure 12, elements 1248 and 1250; the write ports);

f. a first set of data storage devices capable of storing a first state of said embedded processor, wherein said first state is the state of the embedded processor during the execution of the first program thread (Joy, Figures 3 and 17A, column 8 lines 27-44, The register file, or window, of the thread contains the state, information and data of the thread.);

g. a second set of data storage devices capable of storing a second state of said embedded processor, wherein said second state is the state of the embedded processor during the execution of the second program thread (Joy, Figures 3 and 17A, column 8 lines 27-44, The register file, or window, of the thread contains the state, information and data of the thread. Figure 8 shows the cache being shared by the two threads, but in different sections. Each thread operates independently, and has its own individual data storage. Figure 5);

h. wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored wherein at least one of said first or said second target set of data storage devices is not included in the first set of data storage devices (Joy, abstract, Figures 13 and 17A, column 27 lines 15-40, column 29 line 54-columun 30 line 9; Joy has taught cross-talk between a plurality of threads by using source and destination registers that are associated with other threads. A window pointer for a thread points to a window of registers where there are "ins" and "outs" of registers from other threads. The outs of one thread are the ins of another thread. Each thread has it's own window of registers at a certain depth. The "outs" positioned register of one thread is at one depth and the "ins" of another thread of the same positioned register is at a different depth. Therefore, the "outs" register, element 1712, specifies an "ins" register, element 1722, which is at a different depth, or different locations, in the array. So, in Figure 4, the current window, element

1710, has a target set of storage devices, element 1720 (specifically 1722). Element 1722 is not included in the first set of storage devices, element 1710.);

i. a thread scheduler for identifying which of said program threads said embedded processor executes (Joy, Figure 6, column 16 line 42-column 17 line 32); and

j. an instruction set including an instruction that overwrites the first control status register when instructions associated with the first set of data storage devices are executed and overwrites the second control status register when instructions associated with the second set of data storage devices are executed (Joy column 8 lines 27-44column 29 lines 15-53, When a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window.);

k. wherein said processor switches between said first and second state in a time period between the end of the execution of a first program instruction in the first thread and the beginning of the execution of a second program instruction in the second thread (Joy, column 8 lines 45-58, An instruction of the first thread finishes executing. The next instruction causes a cache miss, and therefore a context switch. Then an instruction from the second thread executes.);

l. wherein said processor switches between said first and second states by changing a state selection register (Joy, column 14 lines 5-16).

15. Referring to claim 2 Joy has taught the multithreaded computer based system of claim 1, wherein the embedded pipelined processor further includes a peripheral block (Joy, column 21 lines 55-57).

16. Referring to claim 3, Joy has taught the multithreaded computer based system of claim 2, wherein the peripheral block is one of a phase locked loop and a watchdog timer (Joy, column 17 lines 19-32).

17. Referring to claim 4, Joy has taught the multithreaded computer based system of claim 1, wherein the embedded pipelined processor further includes an internal memory unit comprising a flash memory with a shadow static memory (Joy, column 11 lines 48-53, static memory).

18. Referring to claims 5 and 11, Joy has taught a method of executing instructions in a multithread computer based system having at least a first thread associated with a first context including a set of context registers, the method comprising the steps of:

a. selecting the first thread associated with the first context (Joy, abstract, column 8 lines 27-44, column 29 lines 15-53, When a jump to subroutine or return call is made by the thread, the window pointer is updated to point to the new window. column 3 lines 28-56);

b. fetching a first instruction of the first thread which indicates source data registers associated with operands, each operand associated with a context of one of a plurality of threads, the context comprising data registers (Joy, Figure 12, element 1216, column 8 lines 14-26, Figure 17A, "ins" of element 1710);

c. decoding the instruction to determine a second context and source data register associated with a first operand (Joy, Figure 12, element 1214, abstract Figure 17A, column 29 line 54-columun 30 line 9, Joy has taught cross-talk between threads by using source and destination registers that are associated with other threads. Column 30, lines

9-26, A decode step determines a source register will be in the "ins" section of the registers, which is associated with another thread.);

d. executing the instruction on the first operand to produce a result (Joy, Figure 12, elements 1232, 1234, 1236, 1238, 1240, 1242, 1244, 1246); and

e. storing the result in a destination data register associated with a third context of one of a plurality of threads (Joy, Figures 12 and 17A, element 1722, Column 30, lines 9-26, A decode step determines a destination register will be in the "outs" section of the registers, which is associated with another thread.).

19. Referring to claim 6, Joy has taught the method of claim 5, wherein the decoding further comprises decoding the instruction to determine the context and the source data register associated with a second operand, the context associated with the first operand being the first context and the context associated with the second operand being the second context different from the first context (Joy abstract figure 17A, column 29 line 54-columun 30 line 9; Joy has taught cross-talk between threads by using source and destination registers that are associated with other threads.).

20. Referring to claim 7, Joy has taught the method of claim 5, wherein the destination data register is part of a second set of context registers of a second thread different from the first thread (Joy, abstract, figure 17A, column 29 line 54-columun 30 line 9; Joy ha taught cross-talk between threads by using destination registers that are associated with another thread. The results of the instructions that are to be passed on to another thread go to the "outs" registers in the current window, which is associated with another thread.).

21. Referring to claim 8, Joy has taught the method of claim 7, wherein the decoding step further comprises determining the third context of the destination data register for storing the result (Joy, abstract figure 17A, column 29 line 54-columun 30 line 26, Joy has taught cross-talk between threads by using destination registers that are associated with another thread. Since the decode step shows that the destination register will be in the "outs" section of the registers, the destination is associated with another thread).

22. Referring to claim 9, Joy has taught the method of claim 5, wherein the executing includes modifying a control and status register to indicate the context of the first operand being different than the first context (Joy, column 8 lines 27-44, column 29 lines 15-53, When a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window.).

23. Referring to claim 10, Joy has taught the method of claim 9, wherein the executing further includes modifying the control and status register to indicate a context of the destination data register being different than the first context (Joy, column 8 lines 27-44, column 29 lines 15-53, When a jump to subroutine or return call is made by the thread, the window pointer is updated to point to the new window.).

Response to Arguments

24. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the newly explained ground(s) of rejection above.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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